IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:	§
Adrian P. Wise	§ Application No.: Not Yet Known
Filed: February 8, 2001	§ Art Unit: 2783 (anticipated)
For: MULTISTANDARD VIDEO	§ Examiner: Follansbee, J. (anticipated)
DECODER AND DECOMPRESSION	§
SYSTEM FOR PROCESSING	§ Attorney Docket No.:
ENCODED BIT STREAMS INCLUDING	§ 94100422(EP)USC1X1C1D11 PDDD
CIRCUITRY FOR SELECTING TOKENS	§
AND METHODS RELATING THERETO	§

COMMUNICATION - SUBMISSION OF FORMAL DRAWINGS

BOX PATENT APPLICATION Assistant Commissioner of Patents Washington DC 20231

Sir:

Transmitted herewith are 169 formal drawings on 124 sheets.

In the event a fee is due, the Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment to Deposit Account No. 04-1175

Respectfully submitted,

DISCOVISION ASSOCIATES

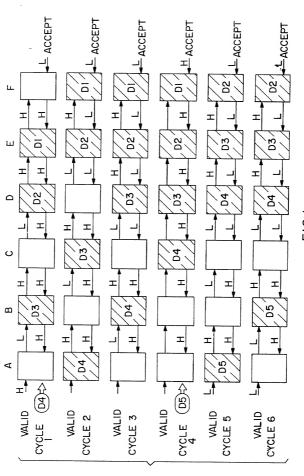
Date: 2/8/01

Richard Stokey Reg. No. 40,383

MISTO

DISCOVISION ASSOCIATES INTELLECTUAL PROPERTY DEVELOPMENT P.O. Box 19616 Irvine, California 92623 (949) 660-5006

RS:sd



F16. I

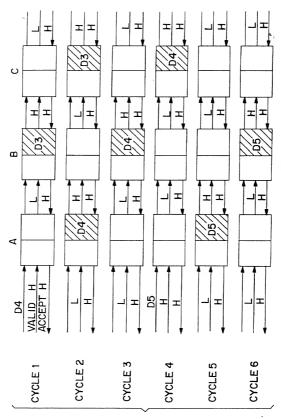
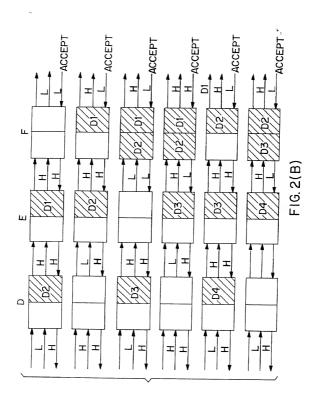


FIG. 2(A)



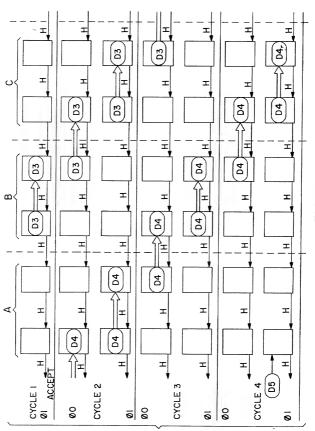
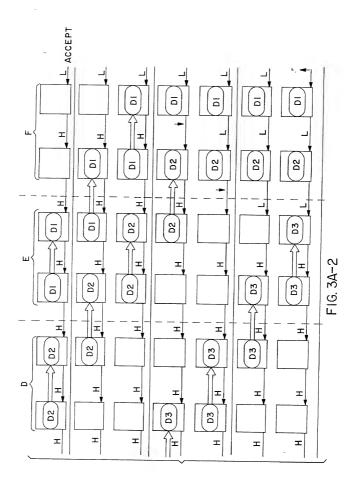
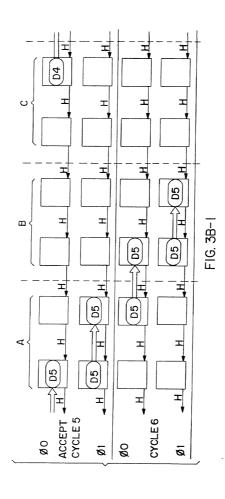
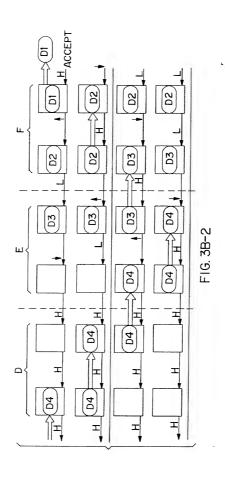
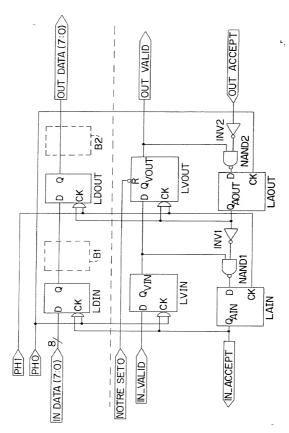


FIG. 3A-1

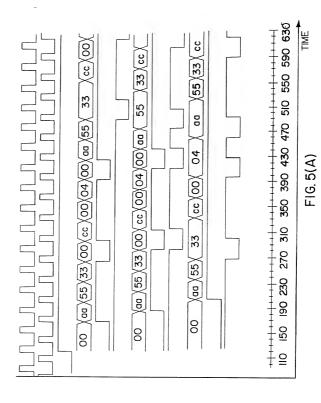


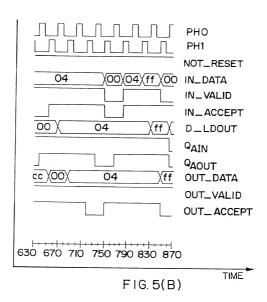






F16.4





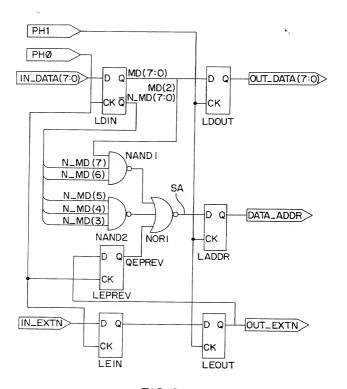
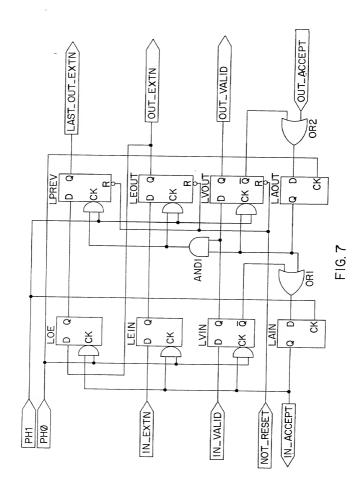


FIG. 6



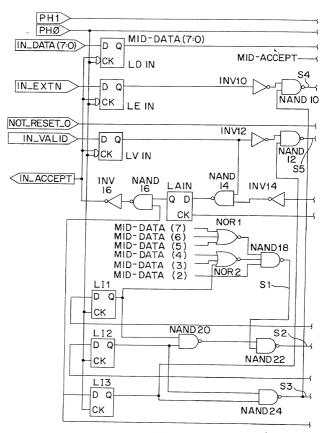


FIG. 8(A)

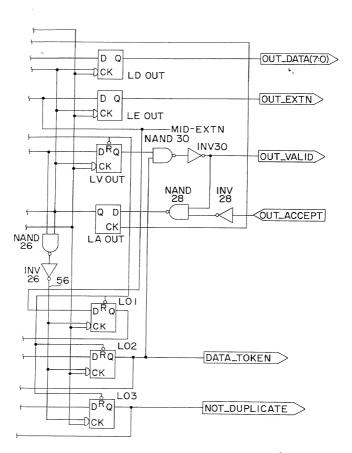
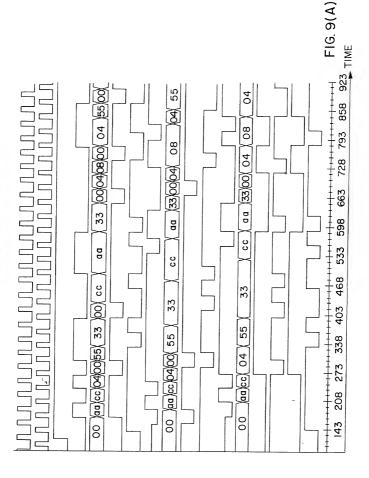


FIG. 8(B)



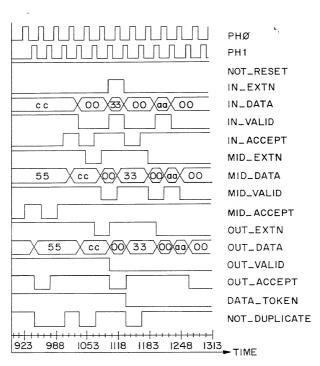


FIG. 9(B)

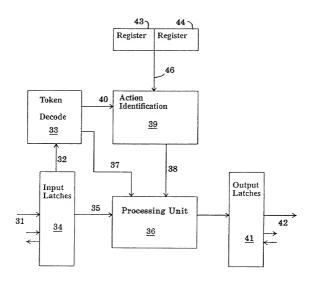
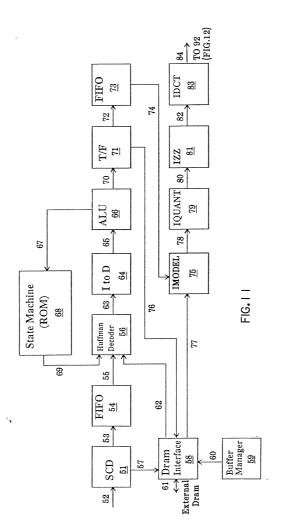


FIG. I O



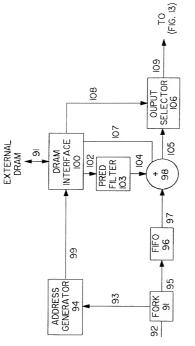
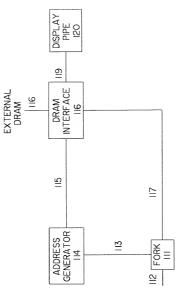
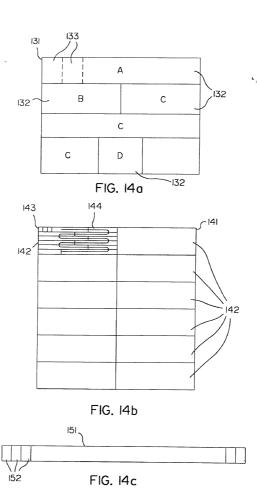


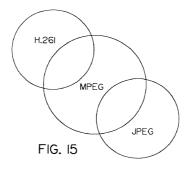
FIG. 12

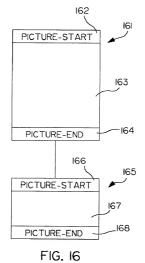
13

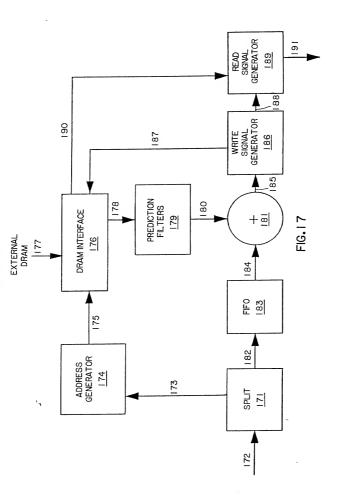


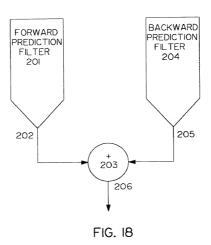
F1G. 13

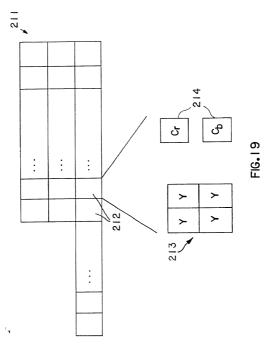


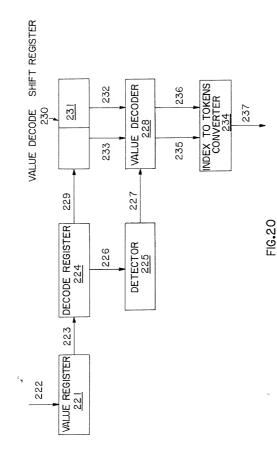


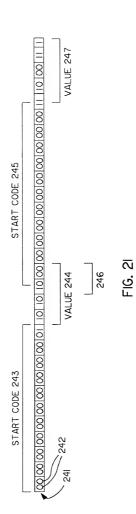












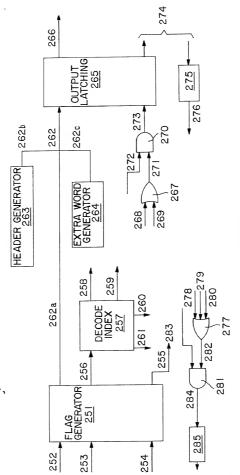


FIG.22

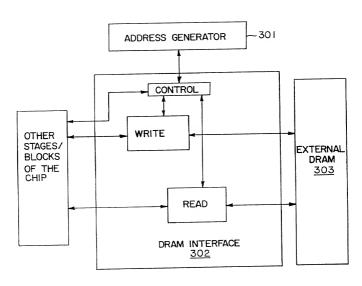


FIG.23

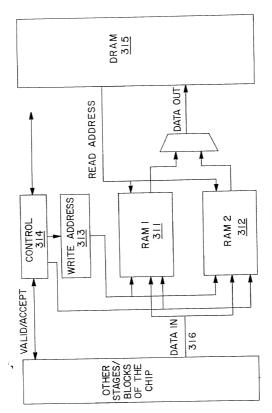


FIG.24

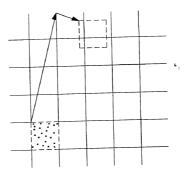


FIG. 25

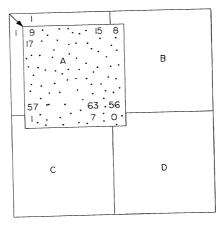


FIG. 26

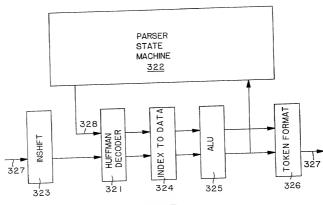


FIG.27

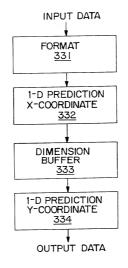
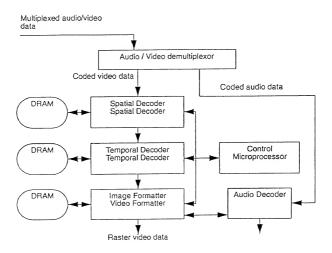


FIG.28



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FIG.29



FIG.30

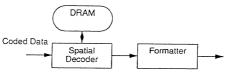


FIG.3 I

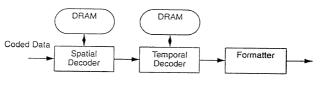


FIG.32

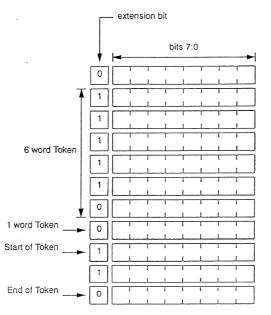


FIG.33

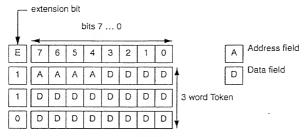
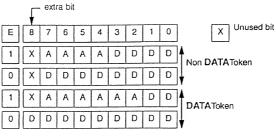


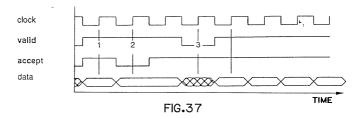
FIG.34



i.

FIG.35





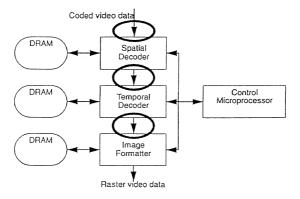
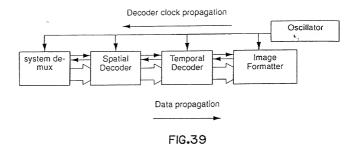
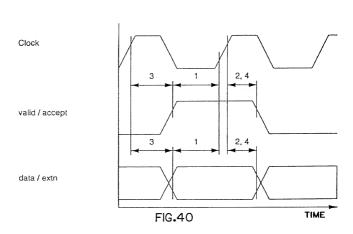


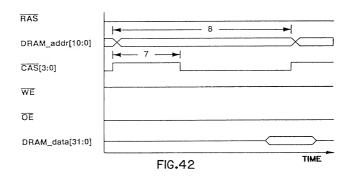
FIG.38

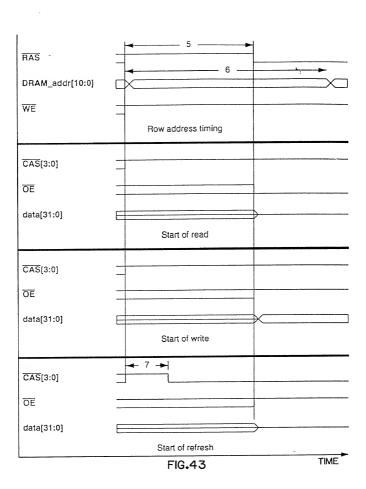


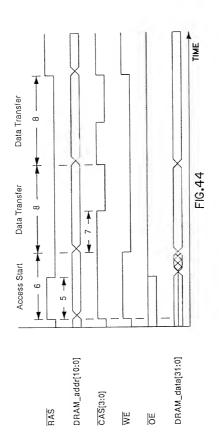


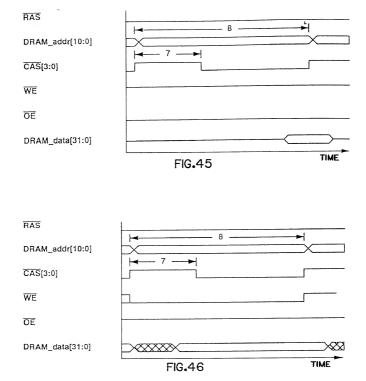
Access Start Data Transfer Default State

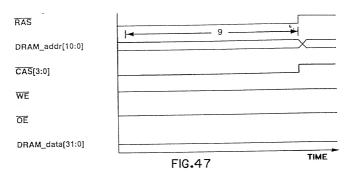
FIG.41











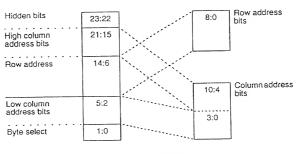
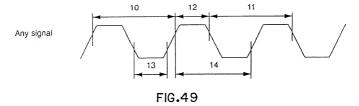
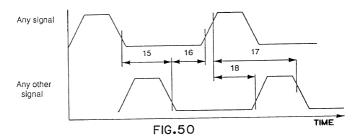
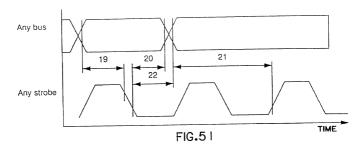


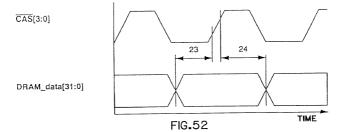
FIG.48



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data[7:0]

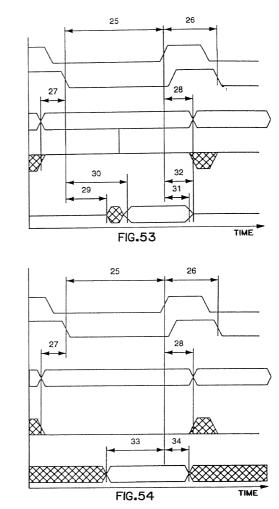
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addr[9:0]

data[7:0]

rw

rw



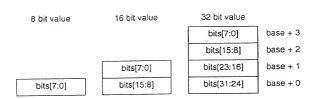
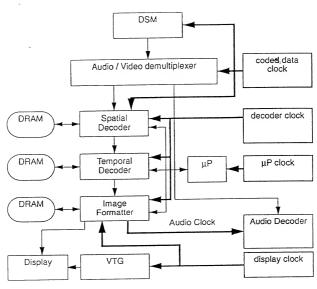


FIG.55





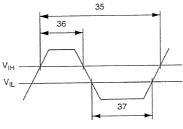
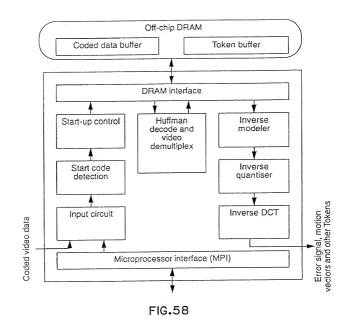


FIG.57



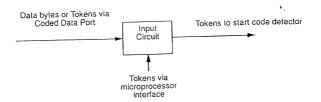
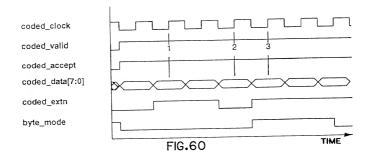


FIG.59



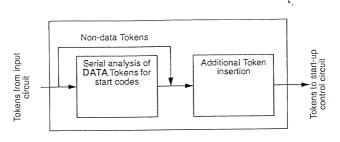


FIG.61

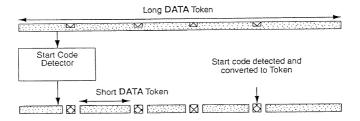


FIG.62

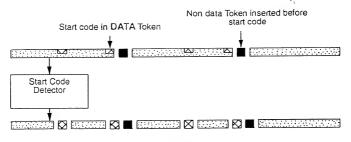


FIG.63



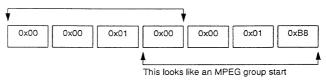


FIG.64

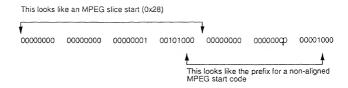


FIG.65

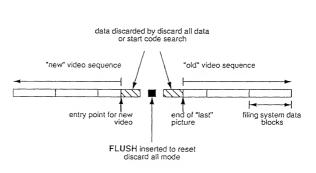
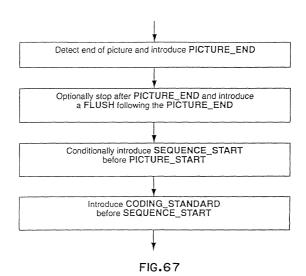


FIG.66



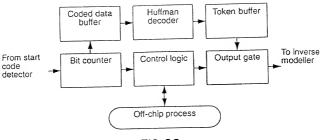


FIG.68

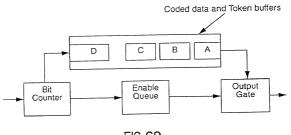
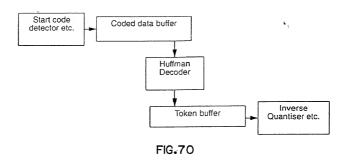


FIG.69



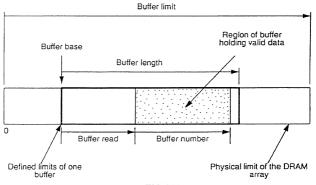


FIG.7 I

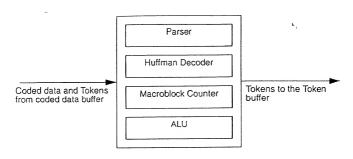
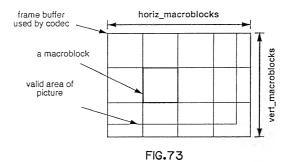
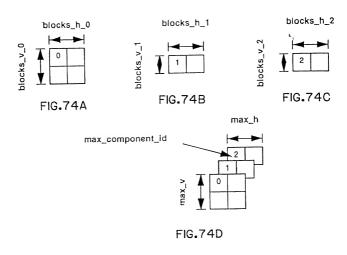


FIG.72

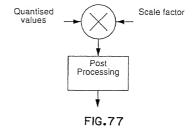




$$\begin{cases} \text{horiz_macroblocks} = \frac{\text{horiz_pels} + 15}{16} \\ \text{vert_macroblocks} = \frac{\text{vert_pels} + 15}{16} \\ \text{FIG.75} \end{cases}$$

From Token buffer Run and Level representation of quantised coefficients Inverse Modeller Expanded to 8x8 blocks of quantised coefficients Inverse Quantiser 8x8 blocks of coefficients Inverse DCT 8x8 blocks of pixel information To output of Spatial Decoder

FIG.76



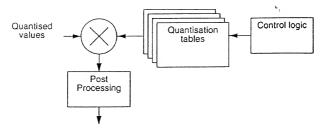


FIG.78

Scale factor

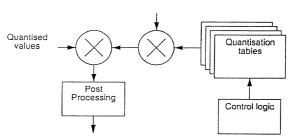


FIG.79

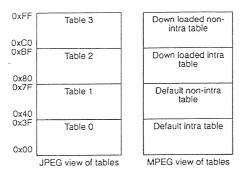
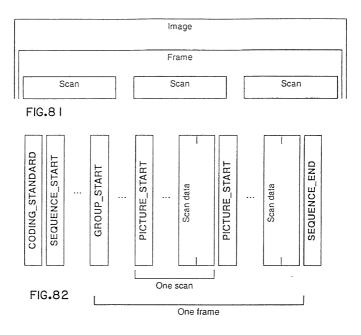
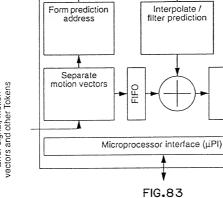


FIG.80





Off-chip DRAM

DRAM interface

Picture

sequence control

Block organised video data and other Tokens

Error signal, motion vectors and other Tokens

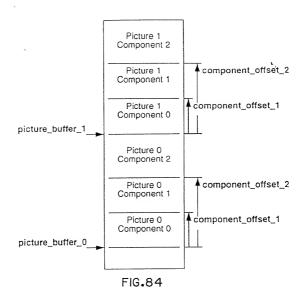
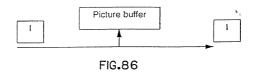
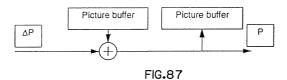
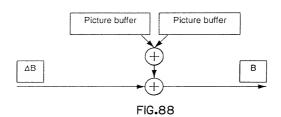




FIG.85







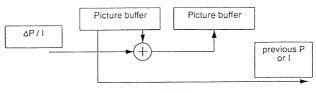


FIG.89

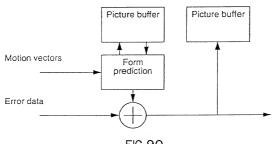


FIG.90

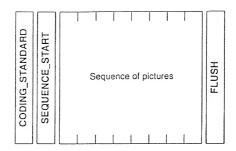


FIG.9 I

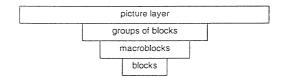
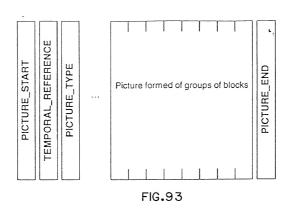
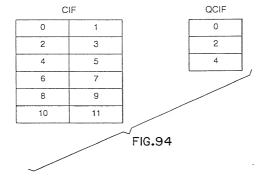


FIG.92





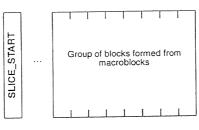


FIG.95

1	2	3	4	5	6	7	8	9	10	11
12	13	14	15	16	17	18	19	20	21	22
23	24	25	26	27	28	29	30	31	32	33

FIG.96



FIG.97

DATA 00	DATA 00	DATA 00	DATA 00	DATA 01	DATA 02		DATA 00	DATA 00	DATA 00	DATA 00	DATA 01	DATA 02	Total Control of the
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FIG.98

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16

59	58	59	60	61	62	63	64

FIG.99

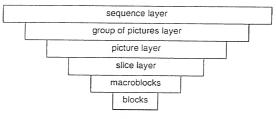


FIG. I 00

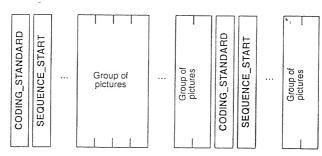


FIG. 101

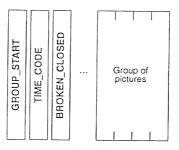
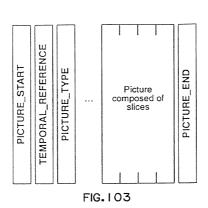


FIG. 102



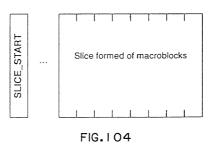


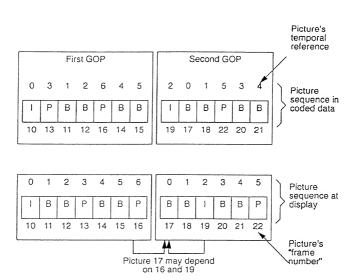


FIG. 105

DATA 00	DATA 00 DATA 00	DATA 00	DATA 01	DATA 02
---------	--------------------	---------	---------	---------

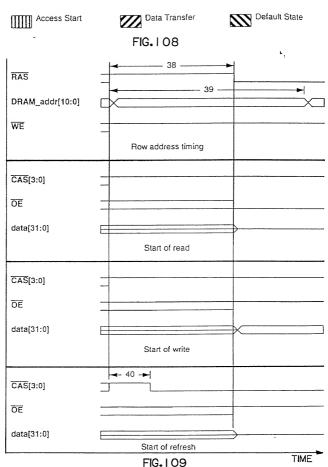
DATA 00	DATA 00	DATA 00	DATA 00	DATA 01	DATA 02
Ω Ω	۵	O O	'a	۵	۵

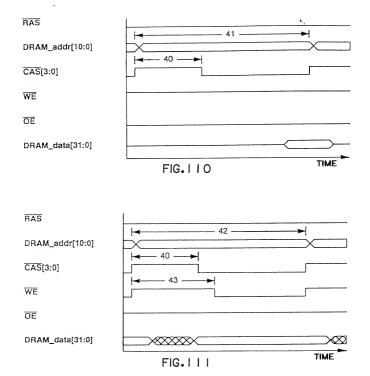
FIG. 106

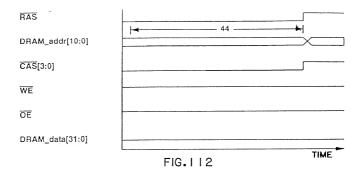


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FIG. 107







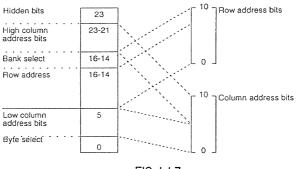
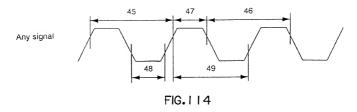
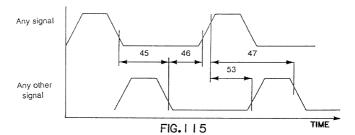
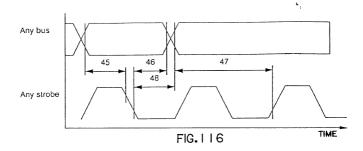
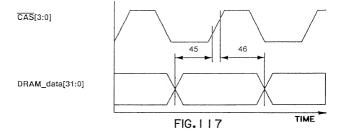


FIG. 1 13









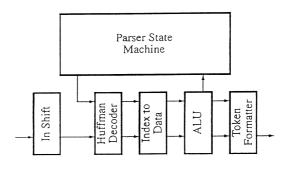
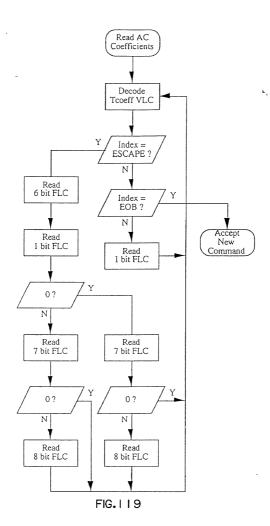
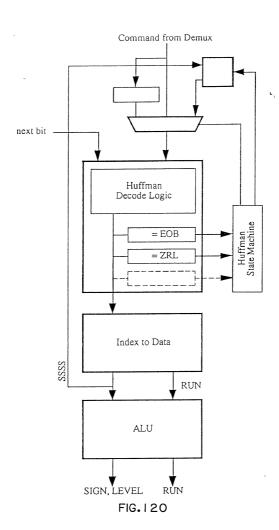


FIG. 118





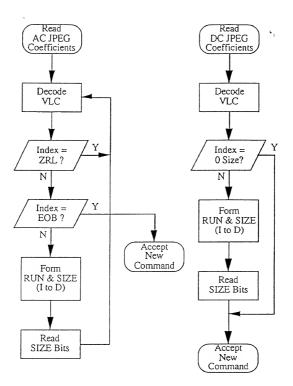


FIG. 121A

FIG. 121B

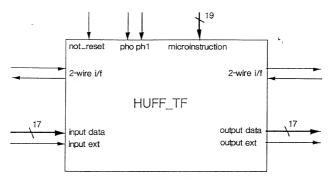


FIG. 122

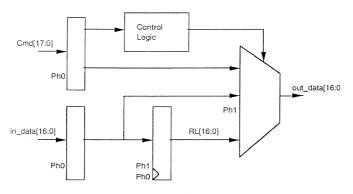


FIG. 123

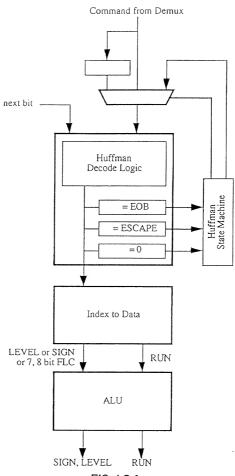
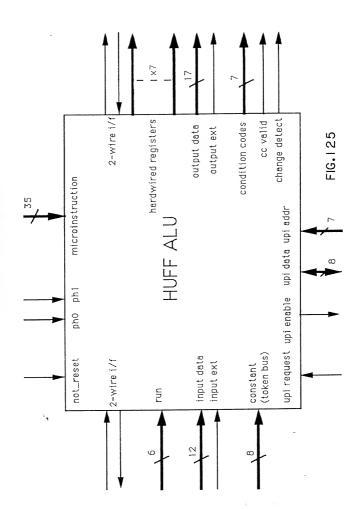
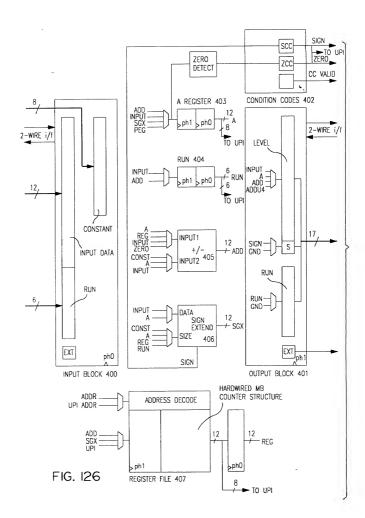


FIG. 124





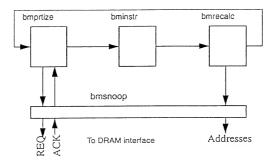


FIG. 127

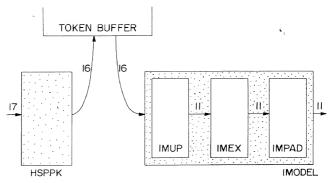


FIG. 128

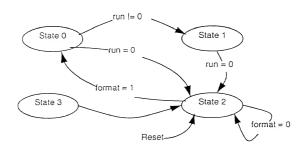


FIG. 129

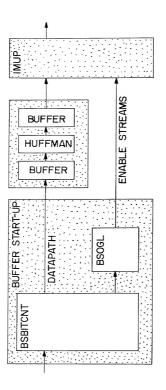


FIG. 130

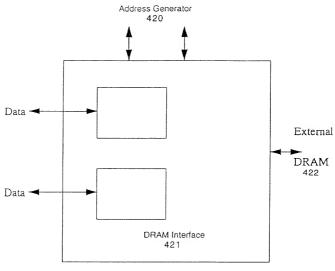


FIG. 131

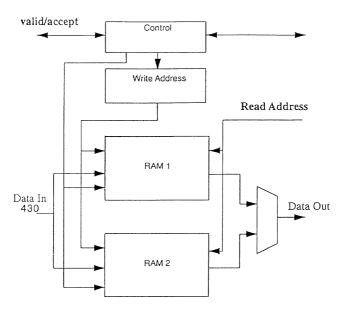


FIG. 132

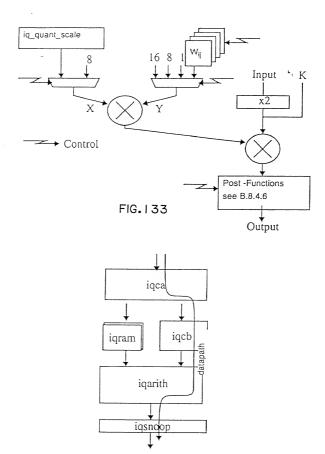
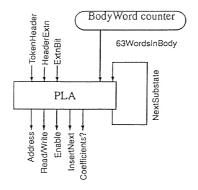


FIG. 134



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FIG. 135

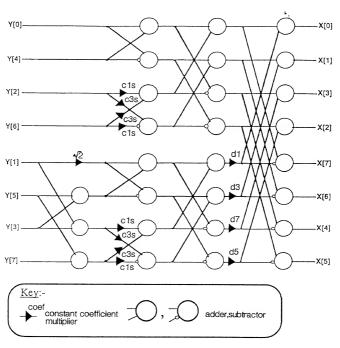


FIG. 136

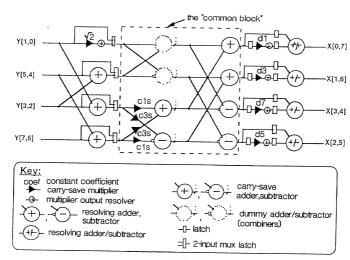


FIG. 137

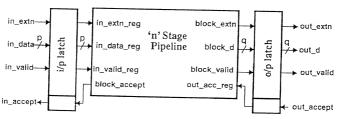
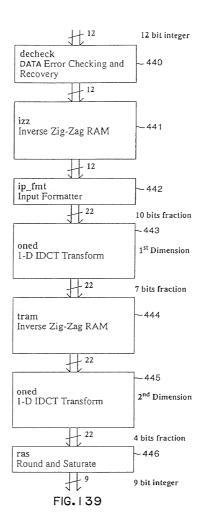


FIG. 138



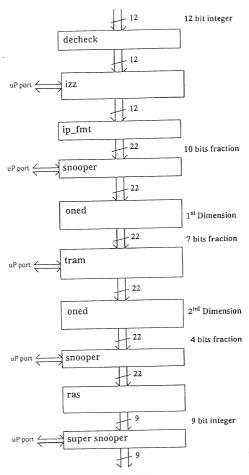
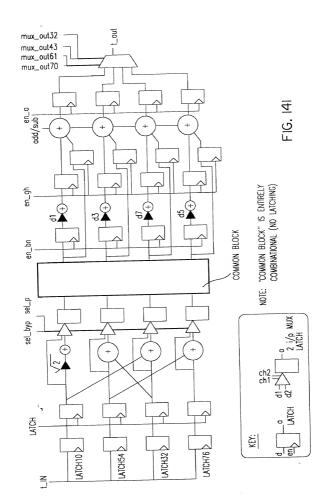


FIG. 140



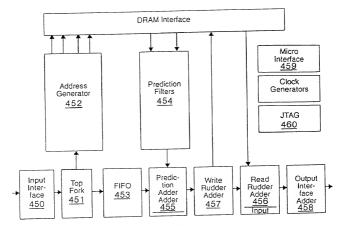


FIG. 142

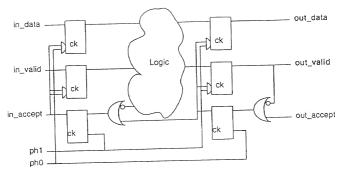


FIG. 143

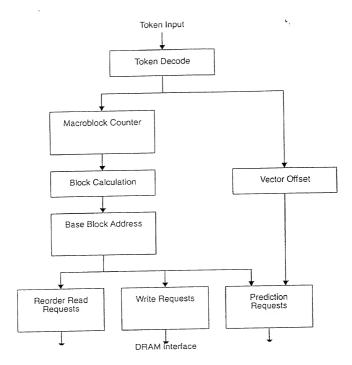


FIG. 144

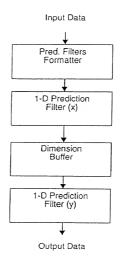


FIG. 147

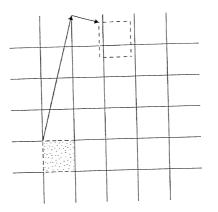
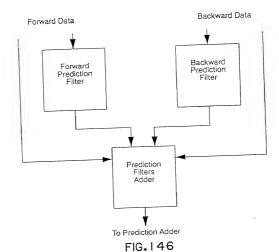


FIG. 145



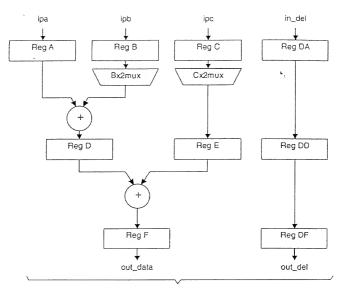
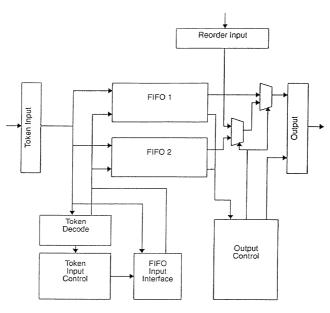


FIG. 148

0	1	2	3	4	5	6	7
8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39
40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55
56	57	58	59	60	61	62	63

FIG. 149



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FIG. 150

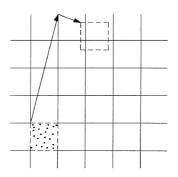


FIG. 151

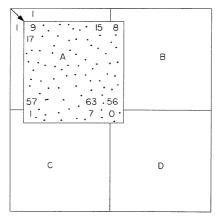
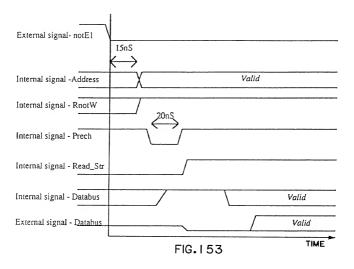
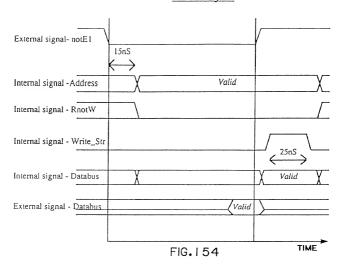


FIG. 152

Read Cycle



Write Cycle



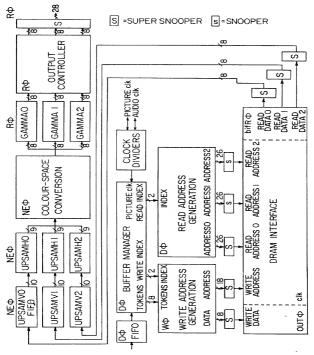


FIG. 155

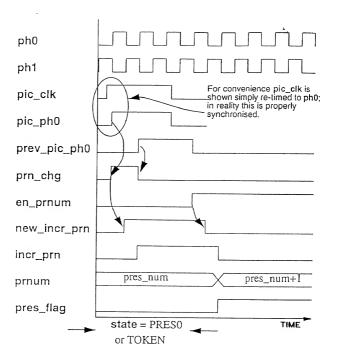


FIG. 156

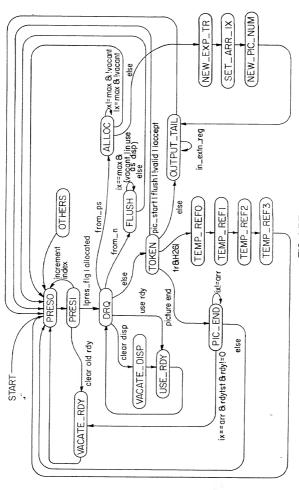


FIG. 157

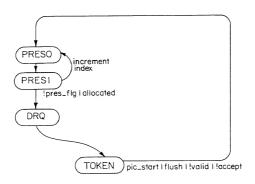
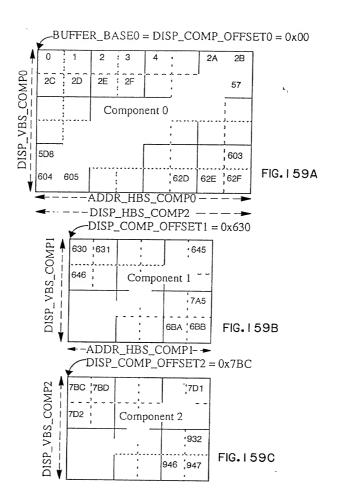
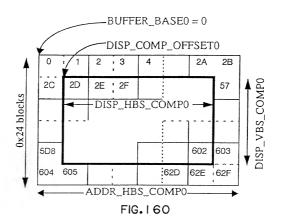


FIG. 158





BUFFER OFFSET 0x00

COMPONENT O	FFSET (000×C	+	
-------------	---------	-------	---	--

00	01	02	03	04	05	06	07	08	09	OA	OB
OC	OD	0E	OF	10	11	12	13	14	15	16	17
18	19	1A	1B	1C	1D	1E	1F	20	21	22	23
24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
30	31	32	33	34	35	36	37	38	39	3A	3B
3C	3D	3E	3F	40	41	42	43	44	45	46	47
48	49		4B						51		53
										52 5E	
54	55	56		58	59	5Ā	5B	5C			
54	55	56 62	57	58 64	59	5Ā	5B	5C	5D	5E	5F
54 60	55 61	56 62	57 63	58 64	59 65 71	5A 66	5B 67 73	5C 68	5D 69	5E 6A	5F

FIG. 161A

COMPONENT1 OFFSET 0x100 +

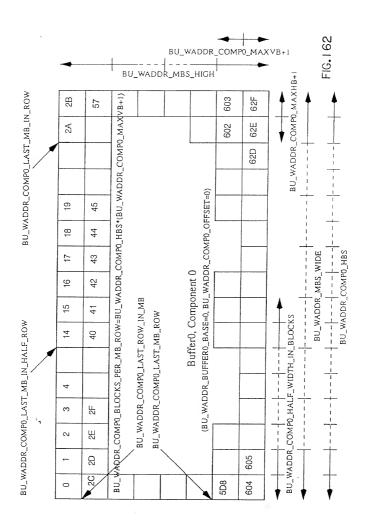
C	00	01	02	03	04	05
C	6	07	08	09	OA	OВ
C	C	OD	ΟE	OF	10	11
1	2	13	14	15	16	17
1	8	19	1A	1B	1C	1D
[1	Ē	1F	20	21	22	23

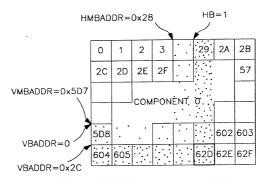
FIG. 16 1B

COMPONENT1 OFFSET 0x200 +

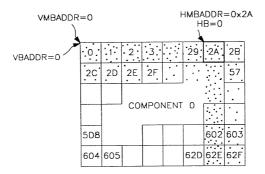
00	01	02	03	04	05
06	07	08	09	OA	OB
OC	OD	0E	OF	10	11
12					
18	19				
1E	1F	20	21	22	23

FIG. 161C

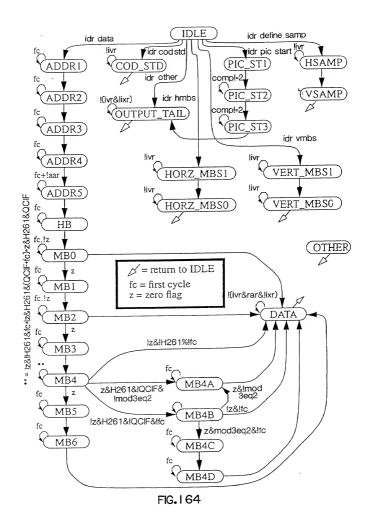


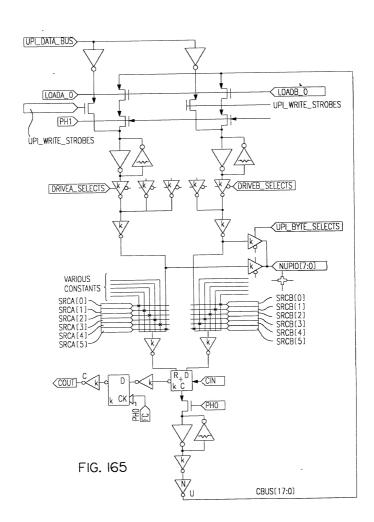


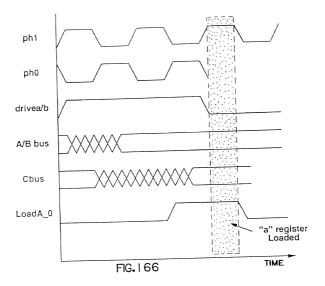
BLOCK ADDRESS=0+0+0x5D8+0x28+0x2C+1=0x62D FIG. I 63A



BLOCK ADDRESS=0+0+0+0x2A+0+0=0x2A FIG. I 63B







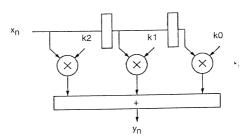
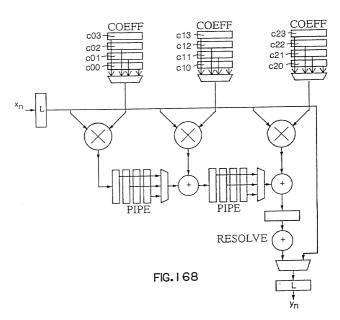


FIG. 167



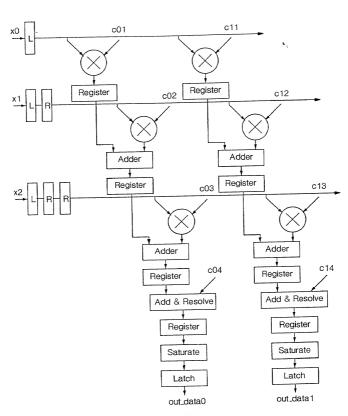


FIG. 169